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EXAMINER	
MOLINARI, MICHAEL J	

ART UNIT	PAPER NUMBER
2665	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/540,878	KUROIWA ET AL.	
	Examiner	Art Unit	
	Michael J Molinari	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,10-19,21,22,24-27,29,31-40,43,44,47,48 and 53-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *47,48 and 62-64* is/are allowed.

6)☒ Claim(s) *2, 3, 7, 10, 11, 13, 14, 16-18, 21, 22, 24-27, 29, 31-33, 35-39, 43, and 53-61* is/are rejected.

7)☒ Claim(s) *4-6,8,12,15,19,34,40 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 2, 3, 7, 10, 11, 14, 16, 18, 21, 22, 24-27, 29, 31, 32, 35-38, 43, and 53-61 are rejected under 35 U.S.C. 102(e) as being anticipated by Higuchi et al. (U.S. Patent No. 6,167,037).

3. Referring to claim 53, Higuchi et al. disclose a cell search method comprising the steps of: detecting correlation values (maximum correlation values) between an input signal and a spreading code (see column 11, lines 31-37); comparing each of said detected correlation values with a threshold value (see column 11, lines 49-62); and detecting a correlation peak value in a predetermined unit of slots in accordance with a result of said comparison (see column 11, lines 45-48).

4. Referring to claim 2, Higuchi et al. disclose that a correlation value exceeding said threshold value is stored in a memory (see column 11, lines 46-48).

5. Referring to claim 3, Higuchi et al. disclose that timing data on the timing at which said correlation value exceeds said threshold value is stored in memory (see column 11, lines 46-48).

6. Referring to claim 7, Higuchi et al. disclose that said threshold value can be arbitrarily set (see column 5, lines 20-23).

7. Referring to claim 54, Higuchi et al. disclose a communication synchronization apparatus comprising: a detection device that detects correlation values between an input signal and a spreading code generated by the detection device (see column 11, lines 30-48), and detects a correlation peak value in a predetermined unit of slots to detect a synchronization point of said input signal (see column 11, lines 46-48), and a comparison section for comparing each of the detected correlation values with a predetermined threshold value (see Figure 9).

8. Referring to claim 10, Higuchi et al. disclose a first storage section for storing a correlation value exceeding said threshold value, obtained as a result of comparison by said comparison section (see column 11, lines 46-48 and see Fig. 9, #S2200).

9. Referring to claim 11, Higuchi et al. disclose a second storage section for storing timing data on the timing at which said correlation value exceeds the threshold value (see column 11, lines 46-48 and see Fig. 9, #S2200 and note that the information stored in memory contains timing information).

10. Referring to claim 14, disclose a register for arbitrarily setting said threshold value (see column 5, lines 20-23).

11. Referring to claim 16, Higuchi et al. disclose an end notification section for notifying the completion of the detection process for said correlation peak value when the detection process is completed (see column 5, lines 14-19).

12. Referring to claim 18, Higuchi et al. disclose a registration count notification section for notifying the number of correlation values stored in said first storage section (see column 11, lines 65-67 and column 12, lines 1-6).

13. Referring to claim 55, Higuchi et al. disclose a computer-readable storage medium for a communication synchronization apparatus comprising: a detection device that detects correlation values between an input signal and a spreading code generated by the detection device (see column 11, lines 30-48), and detects a correlation peak value in a predetermined unit of slots to detect a synchronization point of said input signal (see column 11, lines 46-48), said medium storing a program for causing a computer to realize a comparison function of comparing each of the detected correlation values with a predetermined threshold value (see column 11, lines 31-62 and Figure 9).

14. Referring to claim 21, Higuchi et al. disclose a program for causing said computer to realize a control function of controlling to store a correlation value exceeding said threshold value, obtained as a result of comparison by said comparison function, in a memory (see column 11, lines 30-62).

15. Referring to claim 22, Higuchi et al. disclose a program for causing said computer to realize a control function of controlling to store timing data on the timing at which said correlation value exceeds said threshold value, in a memory (see column 11, lines 30-62).

16. Referring to claim 56, Higuchi et al. disclose a cell search method comprising the steps of: detecting correlation values between an input signal and a spreading code; comparing each of said detected correlation values with a threshold value; detecting a correlation peak value in a predetermined unit of slots in accordance with a result of said comparison; providing a first

mode in which the process is ended when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count set value (see column 11, lines 30-62), and a second mode in which the process is performed a predetermined number of times (see column 11, lines 30-62, which shows that if the threshold is exceeded, then the process stops, otherwise all values are tried and the one with the highest correlation value is chosen).

17. Referring to claim 24, Higuchi et al. disclose that the comparison to check whether an integrated correlation value has reached said reference set value, is performed on the basis of power values (see column 19, lines 63-67 and column 20, lines 1-4).

18. Referring to claim 25, all operations performed by computers are performed on the basis of voltage values, therefore performing a comparison check on the basis of voltage values is inherent in a system such as that of Higuchi et al.

19. Referring to claim 26, Higuchi et al. disclose that said reference set value can be arbitrarily set (see column 5, lines 20-23).

20. Referring to claim 27, Higuchi et al. disclose that said path count set value can be arbitrarily set (see column 5, lines 14-23 and column 11, lines 30-62).

21. Referring to claim 57, Higuchi et al. disclose a cell search method comprising the steps of: detecting correlation values between an input signal and a spreading code (see column 11, lines 31-37); comparing each of said detected correlation values with a threshold value (see Figure 9); detecting a correlation peak value in a predetermined unit of slots in accordance with a result of said comparison (see column 11, lines 46-48); providing a first mode in which the process is ended when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count set value, and a second mode in which the process is

performed a predetermined number of times (see column 11, lines 30-62, which shows that if the threshold is exceeded, then the process stops, otherwise all values are tried and the one with the highest correlation value is chosen).

22. Referring to claim 29, Higuchi et al. disclose that said first and second modes can be arbitrarily selected and set (see column 11, lines 30-62 and note that the modes are arbitrarily selected depending on whether any values exceed the threshold and are arbitrarily set depending on how long it takes to find a value that exceeds the threshold).

23. Referring to claim 58, Higuchi et al. disclose a communication synchronization apparatus comprising: a detection device that detects each slot in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device, the detection process for correlation value is performed over several slots, the correlation values obtained in the slots are integrated to detect a correlation peak value, and thereby a synchronization point of said input signal is detected; and a comparison section for comparing each of a calculated integrated correlation value with a reference set value (see column 11, lines 30-62 and Figure 9).

24. Referring to claim 31, Higuchi et al. disclose a count section for counting the number of paths at which an integrated correlation value has reached said reference set value, obtained as a result of comparison by said comparison section (see column 11, lines 30-62 and note that the apparatus of Higuchi et al. determines the number of paths to be either 1 (when the threshold is exceeded and the value selected) or 0 (if the threshold is not exceeded)).

25. Referring to claim 32, Higuchi et al. disclose that integration is ended when the count by said count section reaches a path count set value (the total number of long codes in the system, see column 11, lines 30-62).

26. Referring to claim 35, Higuchi et al. disclose that comparison by said comparison section is performed on the basis of power values (see column 19, lines 63-67 and column 20, lines 1-4).

27. Referring to claim 36, all operations performed by computers are performed on the basis of voltage values, therefore performing a comparison check on the basis of voltage values is inherent in a system such as that of Higuchi et al.

28. Referring to claim 37, Higuchi et al. disclose that said comparison section compares an integrated correlation value output from an adder for performing integration, with said reference set value (see Fig. 5, #13).

29. Referring to claim 38, Higuchi et al. disclose that said comparison section compares an integrated correlation value output from a memory for storing calculated integrated correlation values, with said reference set value (see column 11, lines 30-62).

30. Referring to claim 43, disclose a register for arbitrarily selecting and setting said first and second modes (see column 11, lines 30-62, which shows that if the threshold is exceeded, then the process stops, otherwise all values are tried and the one with the highest correlation value is chosen).

31. Referring to claim 59, Higuchi et al. disclose a communication synchronization apparatus comprising: a detection device that detects each slot in a predetermined unit, correlation values between an input signal and a spreading code generated by the detection device, the detection process for correlation value is performed over several slots, the correlation values obtained in the slots are integrated to detect a peak correlation value, and thereby a synchronization point of said input signal is detected; and a comparison section for comparing each of the detected correlation value or each of a value output from a power conversion device for converting the

correlation value into a power value, with a reference set value (see column 11, lines 30-62 and see Figure 9).

32. Referring to claim 60, Higuchi et al. disclose a communication synchronization apparatus comprising: a detection device that detects each slot in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection process for correlation value is performed over several slots, the correlation values obtained in the slots are integrated to detect a correlation peak value, and thereby a synchronization point of said input signal is detected; and a first mode in which integration is ended when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count set value, and a second mode in which integration is performed a predetermined number of times (see column 11, lines 30-62 and see Figure 9).

33. Referring to claim 61, Higuchi et al. disclose a computer-readable storage medium for a cell search operation comprising: a detection device that detects each slot in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device, the detection process for correlation value is performed over several slots, and the correlation values obtained in the slots are integrated to detect a correlation peak value, said medium storing a program for causing a computer to realize a function of ending integration when the number of paths at which an integrated correlation value has reached a reference set value, reaches a path count value (see column 11, lines 30-62 and Figure 9).

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (U.S. Patent No. 3,680,055).

36. Referring to claim 17, Higuchi et al. differ from claim 17 in that they fail to disclose an overflow notification section for notifying a shortage of storage area in at least one of said first and second storage sections when it occurs. However, overflow notification mechanisms are well known in the memory art. For example, Wilson discloses the use of an overflow notification mechanism (see column 5, lines 54-69), which has the advantage of preventing data loss. One skilled in the art would have recognized the advantage of an overflow notification mechanism as taught by Wilson. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate an overflow notification mechanism as taught by Wilson into the invention of Higuchi et al. to achieve the advantage of preventing data loss.

37. Claims 13, 33, 39, 47 and 62-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi et al. (U.S. Patent No. 6,167,037) in view of Shibata et al. (U.S. Patent No. 6,115,725).

38. Referring to claim 13, Higuchi et al. differ from claim 13 in that they fail to disclose that said first and second storage sections are provided in a single memory. However, it is old and well known in the art to store more than one value in the same memory. For example, Shibata et

al. teach storing a plurality of values in a single memory (see column 5, lines 37-49), which has the advantage of reducing cost. One skilled in the art would have recognized the advantage of storing a plurality of values in a single memory as taught by Shibata et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate storing a plurality of values in a single memory as taught by Shibata et al. into the invention of Higuchi et al. to achieve the advantage of reducing cost.

39. Referring to claim 33, Higuchi et al. differ from claim 33 in that they fail to disclose a register for arbitrarily setting said reference set value. However, the use of registers for storing values in such a system is old and well known in the art. For example, Shibata et al. disclose the use of registers for storing values, which has the advantage of providing a means of quickly accessing the reference set value. One skilled in the art would have recognized the advantage of using a register to store a reference set value as taught by Shibata et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of a register for storing a reference set value as taught by Shibata et al. into the invention of Higuchi et al. to achieve the advantage of providing a means of quickly accessing the reference set value.

40. Referring to claim 39, Higuchi et al. differ from claim 39 in that they fail to disclose a register for arbitrarily setting said reference set value. However, the use of registers for storing values in such a system is old and well known in the art. For example, Shibata et al. disclose the use of registers for storing values, which has the advantage of providing a means of quickly accessing the reference set value. One skilled in the art would have recognized the advantage of using a register to store a reference set value as taught by Shibata et al. Therefore, it would have

been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of a register for storing a reference set value as taught by Shibata et al. into the invention of Higuchi et al. to achieve the advantage of providing a means of quickly accessing the reference set value.

41. Referring to claim 62, Higuchi et al. disclose a communication synchronization apparatus for performing a cell search operation comprising: a detection device that detects a correlation value between an input signal and a spreading code generated by the detection device, and detects a correlation peak value in a predetermined unit of slots (see column 11, lines 30-62). Higuchi et al. differ from claim 62 in that they fail to disclose a dynamic RAM as a memory used in said cell search operation. However, it is well known in the art to use DRAM in circuits for use determining similarity between values. For example, Shibata et al. teach just such a use for DRAM (see column 5, lines 37-49), which has the advantage of being less expensive than other types of memory. One skilled in the art would have recognized the advantage of using DRAM as taught by Shibata et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of DRAM as taught by Shibata et al. into the invention of Higuchi et al. to achieve the advantage of reducing cost.

42. Referring to claim 47, Higuchi et al. disclose storing integration results from said cell search operation. Higuchi et al. differ from claim 47 in that they fail to disclose a dynamic RAM as a memory used in said cell search operation. However, it is well known in the art to use DRAM in circuits for use determining similarity between values. For example, Shibata et al. teach just such a use for DRAM (see column 5, lines 37-49), which has the advantage of being less expensive than other types of memory. One skilled in the art would have recognized the

advantage of using DRAM as taught by Shibata et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of DRAM as taught by Shibata et al. into the invention of Higuchi et al. to achieve the advantage of reducing cost.

43. Referring to claim 63, Higuchi et al. disclose a communication synchronization apparatus for performing a cell search operation comprising: a detection device that detects each of several slots in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device, and the correlation values obtained in the slots are integrated to detect a correlation peak value (see column 11, lines 30-62). Higuchi et al. differ from claim 63 in that they fail to disclose a dynamic RAM as a memory used in said cell search operation. However, it is well known in the art to use DRAM in circuits for use determining similarity between values. For example, Shibata et al. teach just such a use for DRAM (see column 5, lines 37-49), which has the advantage of being less expensive than other types of memory. One skilled in the art would have recognized the advantage of using DRAM as taught by Shibata et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of DRAM as taught by Shibata et al. into the invention of Higuchi et al. to achieve the advantage of reducing cost.

44. Referring to claim 64, Higuchi et al. disclose a communication synchronization apparatus for performing a cell search operation comprising: a detection device that detects each of several slots in a predetermined unit, a correlation value between an input signal and a spreading code generated by the detection device, and the correlation values obtained in the slots are integrated to detect a correlation peak value, wherein a correlator which detects correlation values in the

slots in the manner of detecting the correlation value in each subunit obtained by dividing said spreading code, storing the correlation values in said memory, and outputting the sum of the correlation values of all subunits (see column 11, lines 30-62). Higuchi et al. differ from claim 64 in that they fail to disclose a dynamic RAM as a memory used in said cell search operation. However, it is well known in the art to use DRAM in circuits for use determining similarity between values. For example, Shibata et al. teach just such a use for DRAM (see column 5, lines 37-49), which has the advantage of being less expensive than other types of memory. One skilled in the art would have recognized the advantage of using DRAM as taught by Shibata et al. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the use of DRAM as taught by Shibata et al. into the invention of Higuchi et al. to achieve the advantage of reducing cost.

45. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi et al. in view of Shibata et al. as applied to claim 62 above, and further in view of Segars (U.S. Patent No. 6,405,321).

46. Referring to claim 48, Higuchi et al. in view of Shibata et al. differ from claim 48 in that they fail to disclose that data access occurs in said dynamic RAM within its refresh cycle. However, it is well known in the art to have data access during the refresh cycle of DRAM. For example, Segars teaches data access during certain times within the refresh cycle of DRAM (see column 4, lines 40-48), which has the advantage of controlling access to the memory. One skilled in the art would have recognized the advantage of data access during certain times within the refresh cycle as taught by Segars. Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to incorporate the access of data within the

DRAM refresh cycle as taught by Segars into the invention of Higuchi et al. in view of Shibata et al. to achieve the advantage of controlling access to the memory.

Allowable Subject Matter

47. Claims 4-6, 8, 12, 15, 19, 34, 40 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

48. Applicant's arguments filed 10 November 2003 have been fully considered but they are not persuasive.

49. Regarding claims 53, 54, 58, and 59 Applicant has argued that Higuchi et al. fail to teach that *each* of the correlation values is compared with the threshold value. However, looking at Figure 9, each maximum correlation value is compared to the threshold value. This process is performed iteratively.

50. Regarding claims 56, 57, 60, and 61, Applicant has argued that, in the present invention, an integration process of a correlation value is ended when the number of paths at which an integrated correlation value has reached a reference set value, a path count set value. However, the examiner has shown above, in rejecting the claims, that Higuchi et al. do teach such a limitation.

51. Regarding claims 60 and 61, Applicant has argued that Higuchi et al. fail to teach integrating the correlation values obtained in the slots. However, Higuchi et al. do teach that

integration is an important part of correlating (see column 10, lines 48-52 as an example, although there are multiple references to the use of integration in calculating a correlation).

52. Regarding claims 58 and 59, Applicant has argued that Higuchi et al. fail to teach comparing each of the calculated integrated correlation value with a reference set value. However, if one reads Higuchi et al. such that only the maximum correlation values correspond to the calculated integrated correlation value (the other correlation values being covered because the claim uses the word comprising) then Higuchi et al. do teach the claimed limitation.

53. Applicant's arguments with respect to claims 13, 17, 18, 33, 39, 47, 48, and 62-64 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J Molinari whose telephone number is (703) 305-5742. The examiner can normally be reached on Monday-Thursday 8am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mjm

Michael Joseph Molinari

ALPUS H. HSU
PRIMARY EXAMINER